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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,377	12/13/2001	Thomas Grassl	GRAS3003/JEK	9840

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EXAMINER	
HOGANS, DAVID L	
ART UNIT	**PAPER NUMBER**
2813	10

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,377	GRASSL, THOMAS	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Amendment B filed on August 1, 2003.

Status of Claims

Claims 1-10 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by 5,426,072 to Finnila.

In reference to Claim 1, Finnila teaches:

- producing vertically integratable circuits comprising producing electrically conductive contacts for vertical integration while producing the integratable circuits, electrically conductive contacts for vertical integration and electrically conductive contacts of the integrated circuit in a continuous process (See columns 3-5 and Figures 1-7)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila.

Claims 2 and 8

Incorporating all arguments of Claim 1 and noting that Finnila teaches forming insulation (13) at places of contact for vertical integration on a front side in a thickness direction of a substrate that will bear vertically integratable circuits (See column 2 lines 44-50 and Figure 2); forming a gap (14b) within the insulation from the front side (See column 3 lines 49-55 and Figure 3); filling the gap with a electroconductive material from the front side to form at least some of the contacts (See columns 3-4 lines 55-05 and Figure 4); exposing the electroconductive material from a rearside opposite the front side of the substrate bearing the vertically integratable circuits at the places of contact for vertical integration (See columns 4-5 lines 14-55 and Figures 5 and 6); applying electroconductive material from the rearside to the previously exposed electric material at the places of contact for vertical integration to form at least some of the contacts (See columns 4-5 lines 14-55 and Figures 5 and 6).

Finnila fails to explicitly teach forming insulation at places of contact for vertical integration on a front side in a thickness direction of a substrate bearing vertically integratable circuits. Noting Applicant's arguments in Paper No. 9, on page 9 first full

paragraph, wherein it is argued that the "insulating layer is applied to the front side of a substrate already bearing a vertically integratable circuit."

However, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the claimed arrangements are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

In light of Applicant's failure to establish the criticality of forming the vertically intergratable circuits before formation of the contacts for vertical integration, it is deemed equivalent to the formation of the contacts for vertical integration and then forming the vertically integratable circuiuts.

Claim 3

Incorporating all arguments of Claims 1 and 2 and noting that Finnila teaches thinning the substrate from the backside before exposure of the electroconductive material from the backside (See columns 4-5 lines 57-30 and Figures 5-6)

Claim 4

Incorporating all arguments of Claims 1, 2 and 3 and noting that Finnila teaches a SOI substrate wherein thinning is performed up to the insulating layer (See columns 4-5 lines 57-30 and Figures 5-6)

Claim 5

Incorporating all arguments of Claims 1, 2 and 3 and noting that Finnila, in columns 4-5 lines 57-30 and Figures 5-6, teaches a SOI substrate wherein thinning is performed up to the insulating layer.

The Examiner notes that Applicant's specification contains no disclosure of either the critical nature of the claimed process (i.e. – thinning until the insulation produced for the contacts for vertical integration is reached) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen processes or upon another variable recited in a claim, the Applicant must show that the chosen processes are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Claim 9

Finnila teaches vertically integratable circuits having electrically conductive contacts (16a) for electrically conductive connection with further vertically integratable circuits (18) comprising electrically conductive contacts (16a) arranged for vertical integration and associated insulations (13) forming part of the vertically integratable circuit, said electrically conductive contacts (16a) having exposed end portions disposed

along opposed front and rear sides in a thickness direction of the vertically integratable circuit. (See columns 3-5 and Figures 1-7). The Examiner notes that the electrically conductive contacts (16a) must have exposed portions on opposing ends, or otherwise, elements 21 and 28 could not be in physical contact with the elements demarcated 16a.

Claim 10

Incorporating all arguments of Claim 9 and noting that Finnila, in Figure 7 shows multiple vertically integratable circuits wherein electrically conductive contacts are connected with each other.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila in view of Silicon Processing for the VLSI Era (2000), volume 1, to Wolf et al.

Incorporating all arguments of Claims 1 and 2 and noting that Finnila fails to explicitly teach wherein the field oxide is produced in a region of the substrate where gaps in the substrate material are completely oxidized.

However, Wolf et al., on pages 268-269, teaches the Deal and Grove model of silicon consumption versus the amount of final oxide thickness. Further, the Deal and Grove model teaches that a finitely thick quantity of silicon can be completely oxidized.

Furthermore, Finnila, in column 3 lines 50-55, teaches forming interconnects in both active regions and field regions so as to provide optimum vertical interconnect placement flexibility.

It would have been obvious to one of ordinary skill in the art to modify Finnila by incorporating a field oxide that is produced in a region of the substrate where gaps in the substrate material are completely oxidized, as taught by Wolf et al., to provide optimum vertical interconnect placement flexibility.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,426,072 to Finnila in view of Semiconductor Manufacturing Technology (2001) to Quirk et al.

Incorporating all arguments of Claims 1 and 2 and noting that Finnila fails to explicitly teach wherein the gaps filled with electroconducive material are performed during production of a metallization level.

However, Quirk et al., on page 301 teaches a copper metallization micrograph courtesy of Integrated Circuit Engineering wherein the vertical interconnects are filled during production of a metallization level. Furthermore, Quirk et al. shows that metallization levels allow for a myriad of possible contacts between successive layers.

It would have been obvious to one of ordinary skill in the art to modify Finnila by incorporating vertical interconnects filled during production of a metallization level, as taught by Quirk et al., to allow for a myriad of possible contact points between successive layers.

Response to Arguments

7. Applicant's arguments filed August 1, 2003, have been fully considered but they are not persuasive.

With regard to Claim 1, the Applicant portends that Finnila fails to teach electrically conductive contacts for vertical integration. The basis for Applicant's argument is that another metal layer (21 or 23) is formed over Finnila's electrically conductive contacts (16a) and, therefore, the electrically conductive contacts (16a) cannot be electrically conductive contacts because another metal layer is formed over them (See Applicant's arguments in Paper No. 9 on page 9 second full paragraph). The Examiner maintains that elements 16a are electrically conductive contacts and that placing another metal layer over top of elements 16a does not change this property.

Additionally, with regard to Claim 1, the Applicant portends that Finnila fails to teach electrically conductive contacts for vertical integration produced in a continuous process. As this argument pertains to matter added in Amendment B, it was not of record at the time of the Non-Final Office Action mailed on May 12, 2003, and does not

require a response. For the sake of expediting prosecution the Examiner deems the process of Finnila to be continuous. The addition of metal layers 21 and 23 do not change the fact that elements 16a are electrically conductive contacts for vertical integration formed in a continuous process for making a vertically integratable circuit. Furthermore, the Examiner notes that the Applicant uses the language "comprising" which is open ended and does not preclude additional processing steps. See MPEP § 2111.03.

With regard to Claim 2, the Applicant proffers that Finnila does not teach wherein the insulating layer is applied to the front side of a substrate already bearing a vertically integratable circuit. The Examiner agrees that the electrically conductive contact for vertical integration, in Finnila, is produced before the integratable circuit is produced. But the Examiner contends that the Applicant has not established the criticality of forming the vertically integratable circuits first. Since Applicant's specification provides no basis or reasoning as to why this sequence of limitations is of importance, it is deemed equivalent to the process patented by Finnila.

With regard to Claims 5, 9 and 10 the Applicant argues matter newly added in Amendment B and, therefore, it was not of record at the time of the Non-Final Office Action mailed on May 12, 2003, and does not require a response.

With regard to Claim 6, the Applicant proffers the same argument put forth for Claim 2. The Examiner refers Applicant to the above response concerning Claim 2.

With regard to Claim 7, the Applicant proffers the same argument put forth for Claim 2. The Examiner refers Applicant to the above response concerning Claim 2.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh
October 16, 2003

Carl D. Whitehead

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